JAPANESE PATENT OFFICE

PATENT JOURNAL

KOKAI PATENT APPLICATION NO. HEI 8[1996]-167703

Technical Disclosure Section

| | | |
|---|---|---|
| Int. Cl.[6]: | H 01 L | 27/108 |
| | | 21/8242 |
| | G 11 C | 11/401 |
| | H 01 L | 27/10 |
| | G 11 C | 11/34 |
| | H 01 L | 25/04 |
| | | 25/18 |
| | H 01 L | 25/04 |

Sequence No. for Office Use: 7735-4M

Application No.: Hei 7[1995]-263382

Application Date: October 11, 1995

Publication Date: June 25, 1996

No. of Claims: 26(Total of 28 pages; OL)

Examination Request: Not requested

# SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF, AS WELL AS A MEMORY CORE CHIP AND A MEMORY PERIPHERAL CIRCUIT CHIP

Inventors: Tomoki Mori
Matsushita Electric
Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka

Ichiro Nakao
Matsushita Electric
Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka

Tsutomu Fujita
Matsushita Electric
Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka

Koji Segawa
Matsushita Electric
Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka

Applicant: 000005821
Matsushita Electric
Industrial Co., Ltd.
1006 Oaza Kadoma
Kadoma-shi, Osaka

Agent: Isao Yamamoto,
patent attorney

[There are no amendments to this patent.]

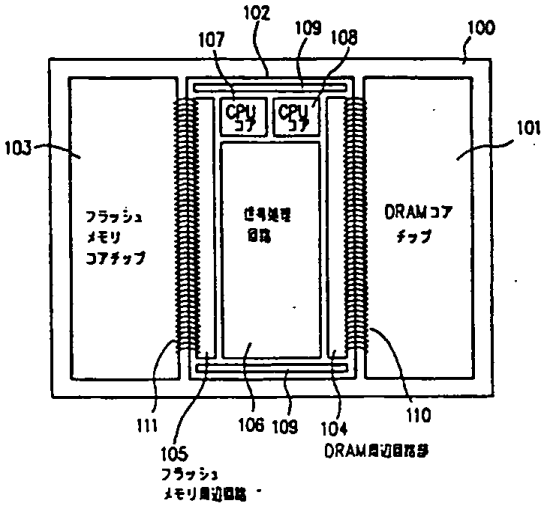
Abstract

Purpose

To provide a low-cost semiconductor device that operates at low voltage and low power consumption.

Constitution

This is a semiconductor device provided with multiple circuit blocks that include a first circuit block (DRAM core) as well as a second circuit block (DRAM peripheral circuit) with different design rules such as the block parameters. The first circuit block is formed on top of a first semiconductor chip (DRAM core chip) 101, and the second circuit block is formed on top of a second semiconductor chip 102 and is electrically connected to the first circuit block. As a result, various low-cost semiconductor chips can be manufactured.




101 DRAM Core Chip
103 Flush memory Core chip
104 DRAM peripheral circuit section

105 Flash memory circuit [section]
106 Signal processing circuit
107 CPU core
108 CPU core

Claims

1. A semiconductor device provided with multiple circuit blocks that include a first circuit block as well as a second circuit block having different design rules such as the block parameters,

said first circuit block is formed on top of a first semiconductor chip,

and said second circuit block is formed on top of a second semiconductor chip and is electrically connected to the first circuit block.

2. The semiconductor device of Claim 1, wherein said block parameters are selected from a group comprising: activation clock frequency, design rules, transistor threshold voltage (Vt), power supply voltage, different parameters of digital circuit or analog circuit, different parameters of standard MOS circuit or CMOS circuit or bipolar circuit or biCMOS circuit, different parameters of ROM or RAM, different parameters of logic or memory.

3. The semiconductor device of Claim 1, wherein said first circuit block is a memory block having multiple memory cells, and said second circuit block is a memory peripheral circuit block for accessing a memory cell selected from said memory cell block.

4. The semiconductor device of Claim 1, wherein said first circuit block is a CPU core, and said second circuit block is a peripheral circuit block.

5. Manufacturing method for a semiconductor device which includes: a step in which the circuits deposited on one semiconductor chip are separated into a first circuit block and a second circuit block having different block parameters;

a step in which said first circuit block is formed on said first semiconductor chip;

a step in which said second circuit block is formed on said second semiconductor chip;

and a step in which said first circuit block and said second circuit block are electrically connected.

6. Manufacturing method for a semiconductor device of Claim 5, wherein said block parameters are selected from a group comprising: activation clock frequency, design rules, transistor threshold voltage (Vt), power supply voltage, different parameters of digital or analog circuits, different parameters of standard MOS circuit or CMOS circuit or bipolar circuit or biCMOS circuit, different parameters of ROM or RAM, different parameters of logic or memory.

7. Manufacturing method for a semiconductor device of Claim 5, wherein said first circuit block is a memory block having multiple memory cells, and said second circuit block is a memory peripheral circuit block for accessing a memory cell selected from said memory cell block.

8. Manufacturing method for a semiconductor device of Claim 5, wherein said first circuit block is a CPU core, and said second circuit block is a peripheral circuit block.

9. A semiconductor device in which the circuits deposited on one semiconductor chip are separated into a first circuit block and a second circuit block having different block parameters, said first circuit block is formed on said first semiconductor chip, said second circuit block is formed on said second semiconductor chip, and said first circuit block and said second circuit block are electrically connected.

10. The semiconductor device of Claim 9, wherein said block parameters are selected from a group comprising: activation clock frequency, design rules, transistor threshold voltage (Vt), power supply voltage, different parameters of digital or analog circuits, different parameters of standard MOS circuit or CMOS circuit or bipolar circuit or biCMOS circuit, different parameters of ROM or RAM, different parameters of logic or memory.

11. A semiconductor device provided with a first circuit section having multiple circuit blocks for the purpose of carrying out at least a first function and a second circuit section having a circuit block for the purpose of carrying out a second function that differs from said first function;

at least one circuit block among the multiple circuit blocks of said first circuit section is formed together with the circuit block of said second circuit section on said first semiconductor chip;

the remaining circuit blocks of said first circuit section are formed on a second semiconductor chip that is different from said first semiconductor chip, and are electrically connected to the circuit block formed on said second semiconductor chip;

and the block parameters for the circuit blocks of said first circuit section formed on said first semiconductor chip are

closer to the block parameters for the circuit block of said second circuit section than to the block parameters for the other circuit block of said first circuit section formed on said second semiconductor chip.

12. The semiconductor device of Claim 11, wherein said first circuit section has at least a memory cell block and a memory peripheral circuit block as the multiple circuit blocks that carry out said first function, said second circuit section has a signal processing circuit as the circuit block that carries out said second function;

said memory processing circuit and said memory peripheral circuit block are formed on said first semiconductor chip, and said memory cell block is formed on said second semiconductor chip.

13. The semiconductor device of Claim 11, for which said block parameters are selected from a group comprising: activation clock frequency, design rules, transistor threshold voltage (Vt), power supply voltage, different parameters of digital or analog circuits, different parameters of standard MOS circuit or CMOS circuit or bipolar circuit or biCMOS circuit, different parameters of ROM or RAM, different parameters of logic or memory.

14. A memory peripheral circuit section chip provided with:

an input/output terminal for sending/receiving signals with respect to another semiconductor memory core chip that includes a memory cell array;

and a memory peripheral circuit that, based upon a provided address, designates a memory cell from said memory cell array within said semiconductor memory core chip, reading or writing data to said memory cell.

15. A memory core chip that is provided with an input/output terminal for sending/receiving signals with respect to another semiconductor chip that includes a memory peripheral circuit; and a memory cell array;

and that, based upon an address that is provided, designates a memory cell from said memory peripheral circuit of said semiconductor chip, reading data from or writing data to said memory cell.

16. A semiconductor memory device provided with at least one memory core section chip formed using a first semiconductor manufacturing process;

a memory peripheral circuit section chip formed using a second semiconductor manufacturing process that is different from said first semiconductor manufacturing process;

and a means to connect said memory core section chip and said memory peripheral circuit section chip.

17. The semiconductor memory device of Claim 16, wherein said memory core section chip includes a memory cell for recording data,

and said memory peripheral circuit section chip, based upon a provided address, designates said memory cell within said memory core section chip, and reads data from or writes data to said memory cell.

18. A semiconductor memory device provided with multiple memory core section chips formed using a first semiconductor manufacturing process;

a memory peripheral circuit section chip formed using a second semiconductor manufacturing process that is different from said first semiconductor manufacturing process;

and a means to connect said multiple memory core section chips and said memory peripheral circuit section chip;

and said memory core section chips shares at least a portion of the circuits on said memory peripheral circuit [section] chip.

19. A semiconductor device provided with at least one memory core section chip, formed using a first semiconductor manufacturing process, that includes a memory cell for recording data;

a signal processing chip that carries a signal processing circuit that performs processing using data recorded on the memory core section chip as well as a memory peripheral circuit section formed using a second semiconductor manufacturing process that is different from said first semiconductor manufacturing process;

and a means to connect said memory core section chip and said signal processing chip.

20. The semiconductor device of Claim 19, wherein said memory peripheral circuit section designates said memory cell on said memory core section chip based upon an address that is provided, and reads data from or writes data to said memory cell.

21. The semiconductor device of Claim 19, wherein there are multiple memory core section chips, and wherein they share at least a portion of the circuits in the memory peripheral circuit chip.

22. A semiconductor device on which is mounted a memory chip as well as a signal processing chip by means of a multichip mounting means, wherein

said memory chip is provided with a memory cell array section having multiple memory cells that store data; an access means that designates said memory cells in said memory cell array

based upon an address that is provided for inputting and outputting data; and a data terminal for inputting/outputting data into rows,

said signal processing chip is provided with a data terminal for inputting/outputting data into rows,

and a means to transmit data to rows is provided between said memory chip and said signal processing chip.

23. The semiconductor device of Claim 22, wherein said memory chip is realized using a first semiconductor manufacturing process,

and said signal processing chip is realized using a second semiconductor manufacturing process that is different from said first semiconductor manufacturing process.

24. The semiconductor device of Claim 22, wherein said signal processing chip is further provided with multiple signal processing circuits.

25. A semiconductor device on which are mounted a memory core section chip as well as a signal processing chip by means of a multichip mounting means,

said memory core section chip is provided with a memory cell array having multiple memory cells that store data and with a data terminal that inputs/outputs data into rows,

said signal processing chip designates said memory cell on said memory core section chip based upon an address that is provided, reads data from or writes data to said memory cell, and is provided with a data terminal that inputs/outputs data into a row, as well as with multiple signal processing circuits,

and a means to transmit data to the row is provided between said memory core section chip and said signal processing chip.

26. The semiconductor device of Claim 25, wherein said memory core section chip is realized using a first semiconductor manufacturing process,

and said signal processing chip is formed using a second semiconductor manufacturing process that is different from said first semiconductor manufacturing process.

* * *